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## ***Design for Boundary Scan Test Board Level DFT***

The appearance of VLSI components contained in smaller packages placed closer together has created new challenges in testing electronic circuit assemblies. Faced with, an increasing number of layers in the PCB, two sided assembly of components, new SMT techniques such as Tape Automated Bonding (TAB), shrunk packages like Ball Grid Arrays (BGAs), pressure for fast product launch and quick delivery, test engineers who are usually the last link in the product delivery chain, find themselves under a continuous pressure to adopt effective test strategies, develop applications quickly, and be expedient in sending good products out of the door. At the test stage, bad design practices that constrain test engineers' tools and hamper the effectiveness of their strategies to provide test coverage can seriously delay product delivery and add to the cost of production.

This document is intended to help design engineers implement boundary scan (IEEE 1149.1) for test and on-board programming of their target assemblies. It aims not only to help design engineers avoid wrong or weak implementations of boundary scan, but also help utilize multifaceted benefits of the boundary scan technique in testing products and programming devices. Where a commitment is made to boundary scan strategy, this document is intended to help prevent engineering changes, which may result if testability is not adequately addressed earlier during the design cycle.

With boundary scan becoming a central piece in many board test and programming applications, attention to DFT and adherence to proper design practices is become essential for successful launch and production of many new products. A methodical approach to implementation of boundary scan on target boards (UUTs) is outlined in the following paragraphs. This approach starts with the selection of components for the target board design. It then continues with configuring the boundary scan chain, following which, issues relating to the distribution of the JTAG (IEEE 1149.1) signals and mixed logic designs are determined and discussed. Then, there are suggestions for conflict management, mechanical connections, and problems that are specifically related to on-board programming of components.

## ? **Selection of IEEE 1149.1 compliant Components**

Clearly, inclusion of a maximum possible number of (IEEE 1149.1) compliant components on the target board will enhance test coverage and diagnostics. Where available, choosing parts that support and comply with IEEE 1149.1 should be taken into consideration. Cost that is sometimes a prohibiting or a limiting factor, should be weighed against the numerous advantages gained specially in test coverage.

Components like microprocessors that provide access to largest areas of the target board **should** be IEEE 1149.1 compliant. Typically, This will help achieve a higher level of fault coverage and better diagnostics. It should also be born in mind that faults on boundary scan nets can be detected where

- a) At least one BScan driver and one BScan receiver cell are connected to the same net
- b) There is a transparent component (a jumper, a resistor, or a buffer) connected in series between a BScan driver/receiver pair. Bi-directional buffers, if used in the design, may enhance diagnostic resolution
- c) At least one BScan driver and one BScan receiver exist on the net, but the net is also connected to one non-scan device lead. It should be possible to disable the non-boundary scan device, and control the pin, especially if the pin is an output. Please refer to the discussion on Critical Nodes outlined below
- d) The nodes are part of the TAP (Test Access Port) circuitry
- e) Nets are connected to logic devices or clusters that are placed between BScan driver/receiver cells, however, depending on the specific application, test coverage and diagnostic capability may be limited

## ? **Chain Configurations**

A simple chain comprises of cascading the TDI and TDO signals of various boundary scan components in the scan chain. The TCK and TMS lines are connected to all components in parallel. Sometimes there is a necessity for more than one chain on the board. Through put, management of different logic and supply levels on the target board, different speed of operation of various BScan devices in JTAG mode, and a requirement for on-board device programming may justify splitting the chain to two or more.

## ? **TCK/TMS Distribution**

If there are a large number of BScan devices on the board (typically more than four to five), it may be necessary to buffer the signals. Buffers may require enables or other conditioning circuitry. Therefore the control of the TAP buffers must be kept as simple as possible. It is also advisable that the designers document the procedure for enabling/disabling the buffers, provide access to nets that control them, and ensure that the IEEE 1149.1 controller and development environment that they are utilizing to perform the tests is readily capable of controlling the enable lines to the buffers. It must always be remembered that due to the way the BScan protocol operates, logical inversion of TCK and TMS is not permitted.

## ? Mixed Logic Families

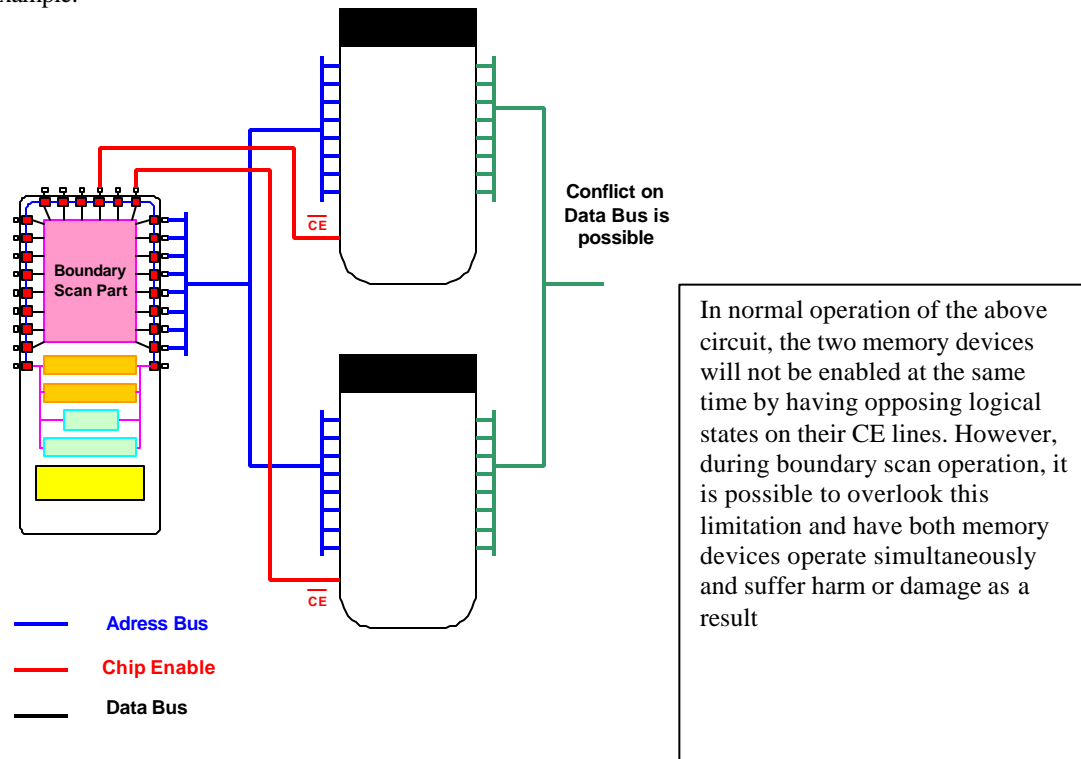
With introduction of lower supply and logic voltage levels for driving digital circuits, it has become increasingly important to ensure that different logic families can be deployed in boundary scan mode. If a single chain is used to connect components from different logic families, voltage converters must be employed in the Test Access Port (TAP) circuitry.

In general, when mixed logic families are used on a printed circuit assembly, level converters for TCK and TMS should be non compliant with IEEE 1149.1 and TDI and TDO should be distributed using IEEE 1149.1 compliant level converters.

## ? Conflicts

Under normal operating conditions, digital electronic circuits have logical limitations on certain nodes that prevent them from conflicts that may be damaging or detrimental to certain components in the assembly. Many of these limitations may be over-ridden or neglected in the BScan mode. Conditions or states of a circuit under BScan operation, not foreseen in the design, can create conflicts that may interfere with the target board operation in a negative way and may even result in damages to the board. The following circuit shows one such example.

Example:



Therefore, it is important to check the conventional (non-BScan) portions of target circuitry that may be affected by BScan test patterns for damaging conflicts. Disabling methods must be designed to protect these sections of the circuit and make them immune to conflicts when test activity is in progress. It is just as important to ensure that boundary scan test tools have the necessary software and hardware facilities to control the relevant nets.

#### ? **Critical Nodes**

1. There are instances when connections of non-boundary scan outputs to boundary scan nets can interfere with testing in which case, the interfering components need to be disabled during test. The ability to disable these components must be designed in, and access to the relevant nets must be provided.
2. In other instances, in order to put certain boundary scan compliant parts into test mode, one or more inputs to the part have to be conditioned to predefined logical states. The design must recognize these requirements and allow for them through providing electrical and physical access to the relevant nets. The boundary scan tool suite must have software and hardware features to facilitate preconditioning. Documenting the pins and the logic states for any devices requiring pre-conditioning is recommended.
3. If TRST pin is implemented on the boundary scan component(s), the means to set this pin to a high state during test must be available and accessible.

#### ? **Power distribution and conflicts with analog sections**

On target boards populated with analog and digital components, interaction of the digital and analog signals may sometimes have undesirable effects on the analog portion of the board during boundary scan test which may sometimes cause damage to the target board, the hardware components in the test tools, and the operator. Therefore, it may become mandatory or advisable to separate the power supply of the critical analog portions of the board from digital sections. The power to analog sections can be switched off while boundary scan test is underway. While, this will compromise test coverage of faults appearing between analog and digital nets, it may be essential for safe testing of the target. Such procedures should be clearly outlined and documented.

#### ? **Post-test conflicts**

Even though boundary scan components will settle internally to safe states after the completion of a test sequence, it should be recognized that assembled circuits may settle into conflicting and possibly damaging states at the end of a test. The reason for this is that assembled PCBs will typically have non-boundary scan parts and therefore it must be ensured that a board will be brought to a safe state on all relevant nodes after the completion of test. Scanning a known safe pattern at the end of the test

usually performs this, however, other methods such as power cycling may also be employed.

## ? **Mechanical connection**

There are electrical and mechanical issues that should be taken into account while designing a board targeted for boundary scan test and/or on-board programming:

### *a) The boundary scan (JTAG) port connection to the test tool*

It is important to ensure that a reliable and easy method is established to connect the vector delivery tool to the target. Acculogic system is configured with different connectors and the information about these connectors is available separately. Depending on the requirements, one of these systems can be adapted to best suit the design. In certain cases, it may also be possible to design special connectors to mate with the connection foreseen on the target board.

### *b) Ground connections*

The ground plane of the target board should be connected to the ground plane of the TAP circuitry.

### *c) Termination of TAP circuitry*

There are provisions in the IEEE 1149.1 standard for connecting the TAP circuitry of UUTs to the hardware of the tool-set. Compliance with the provisions outlined in the following lines will ease the operation of the boundary scan circuitry and will enhance its reliability.

- i) TDI should be pulled high on the target board with a 10k resistor.
- ii) TCK should be terminated with a 50-60 Ohm resistor. To prevent reflections and ringing on the high speed TCK line, it is recommended to foresee installation of an additional small capacitor.
- iii) TMS should be pulled high with a 10k resistor and it is recommended that the provision for installing a high frequency noise filter (as outlined in (ii) above) be maintained.
- iv) TDO can be connected via a 22 to 33 Ohm series resistor to the hardware of the boundary scan hardware tool.
- v) TRST is active low. This line should be pulled high with a 10k resistor.

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## ? **On-Board Programming (OBP) Considerations**

Many devices including Flash, E<sup>2</sup>PROM, Serial PROMS, CPLDs, PLDs can be programmed after assembly using the boundary scan protocols.

In particular, there are certain precautions that will especially enhance boundary scan performance for programming Flash components. The following lines emphasize design practices that will improve performance in on-board programming (OBP) applications where Flash devices are involved;

- a) Connecting the complete address, data and control buses of memory components to boundary scan chain will facilitate testing and programming of these components after assembly (OBP).
- b) Allowing direct and separate access, both physical and electrical, to the control bus of Flash memory devices will allow for much faster OBP. It is best to provide access via a connector or a header if possible.
- c) Keeping the boundary scan chain length required to program the Flash component as short as possible will speed up the programming process and will enhance its reliability.
- d) In configuring scan chains and ear-marking them for Flash programming, attention should be paid to the maximum TCK rate at which each component on the chain can run. For highest through put in Flash programming, it is important to ensure that the TCK frequency of the components on the chain is high. If there are slow components, it may be better to keep them together in a separate chain.

In programming PLDs and CPLDs, designers should ensure that their boundary scan tools will support the protocols demanded by the manufacturers of the PLDs and CPLDs. Major manufacturers of PLDs and CPLDs utilize serial vector format (**SVF rev-c** and **SVF rev-e**) for programming their products. Since there are differences between the vector formats, designers and test engineers must make certain that the boundary scan toolset is compatible with the components that they will program.