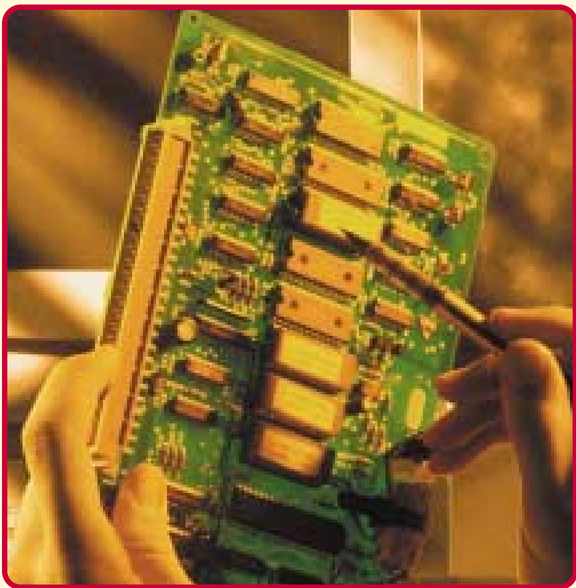
CMP

CIRCUITS ASSEMBLY

Test Strategies


FPG® International

Complementary Test Strategies on High-Complexity Boards

Amit Verma, Mark Ogden and John Kokoska

A combined test approach reduces PCA time-in-process by minimizing debug/repair/retest time.

A key challenge facing electronics manufacturers of high-complexity boards is the issue of board test strategies. An effective board test strategy can be critical in determining a company's ability to succeed in an environment of extreme cost pressures, trends towards smaller components, increased manufacturing complexity, new packaging technologies, higher functionality boards, reduced test access and shorter product life cycles.

Two pillars of survival for an electronics manufacturing services (EMS) provider are asset utilization and inventory turns. Using assets as efficiently as possible to ensure shipment of the highest quality boards at the lowest possible cost is key to maintaining profitability. Time-in-process is a critical factor in this equation; products must get through the manufacturing process in the fastest possible time while minimizing scrap and rework. The more products shipped with current assets while minimizing scrap and rework, the better the asset utilization, the higher the inventory turns and the higher the profitability.

The problems associated with manufacturing printed circuit assemblies (PCAs) become even more difficult as the board's complexity increases. Problems associated with the more complex boards include:

• reduced physical access for in-circuit

test (ICT)
- reduced visual access for human inspectors
- increased complexity of the manufacturing assembly process
- more expensive work-in-process
- more time-consuming and costly ICT fixturing and program development
- more difficult ICT and functional test (FT) diagnostics and repair.

With many high-complexity products having 20,000 or 30,000 solder joints, even the most capable process operating at a very low parts-per-million (ppm) defect rate will exhibit disturbingly low yields, extremely high ICT and FT debug costs, very high cycle times and very low inventory turns.

An effective test strategy maximizes fault coverage at a reasonable or lowest possible cost while meeting cycle time targets. This desired result is becoming increasingly difficult to achieve using only in-circuit and functional testing on high-complexity circuit boards; that is, boards with more than 3,000 nodes and/or 15,000 solder joints. The high value invested in the high-complexity boards requires that these boards move through the manufacturing and test process, including debug and repair, as quickly as possible.

To deal with these issues, an effective test approach is required. Numerous methods exist to test PCAs, including automated optical inspection (AOI), automated x-ray inspection (AXI), ICT, functional test, manual visual inspection, laser paste inspection and environmental stress screening (ESS). However, each test strategy has its own strengths and weaknesses.

Selecting a Test Strategy

Formulating the right test strategy depends on the requirements of the product at hand. One approach is to construct a defect pareto using a defect prediction model. The most effective method of capturing the faults is then determined using a modeling/simulation tool that contains the fault coverage of each test method. Factors that have to be included in the cost model are:

- cost of application development
- capital cost
- throughput
- false fail rate
- false accept rate
- debug times
- fault coverage of the different testers.

A proprietary modeling tool called Quality Modeling System (QMS) optimizes the test strategy on any particular board to meet customer needs (Figure 1). The main input to the model is the customer bill of material (BOM). The board parts are then classified into electrical (SRAM, ASIC, transistor) and physical (0805s, Jleads, ball grid arrays, etc.) categories. Based on historical data, the incoming ppm component quality (electrical defects) can be approximated with the electrical classification; similarly, the assembly defect rates (physical defects) can be estimated with the physical classification.

The output of the combined electrical and physical classifications is the estimated fault spectrum and ppm defect levels based on the customer BOM. The BOM is then analyzed for design rule violations. When a design rule is violated, the ppm defect impact of the violation is approximated. After this analysis, a good approximation of the fault spectrum and the board's defect rates is available.

With this information, the impact of using different test strategies can be modeled. For example, estimates can be made of the impact of using just visual inspection and functional test, AOI with ICT and functional test, and x-ray test with ICT and functional test. Based on this analysis, the optimum test strategy can be determined for the particular board. The model then provides the estimated yields, repair and scrap costs, defects per million opportunities (DPMO), defects per unit (DPU) and other factors. These numbers are used to set production quality targets.

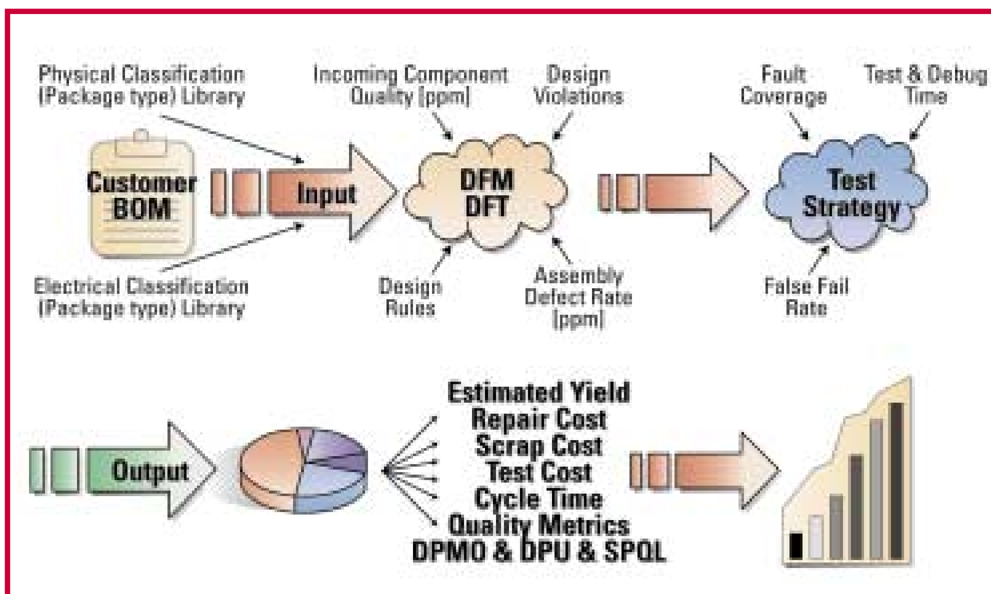


FIGURE 1: Quality Modeling System.

In actual production, the targets are monitored, and action is taken when the targets are not met. To keep the model as accurate as possible, any time there is a noticeable deviation from the model, the reason for the deviation is analyzed. If the model is inaccurate, it is updated to ensure it provides accurate data and targets.

Without a modeling tool like QMS, the high number of choices and convoluted, overlapping coverages of the

✓ >85% Coverage | + 25% to 85% Coverage | ✗ <25% Coverage

	API	HUM	AOI	AXI	FLY	ICT	PCBS	FT	ESS
Bad part	✗	✗	✗	✗	+	+	✓	✓	✓
Wrong part	✗	+	✓	✗	+	✓	✓	✓	✓
BGA Solder	+	✗	✗	+	✗	+	+	+	+
Solder Open	+	+	✗	✓	+	+	+	✓	✓
Solder Short	+	+	+	✓	+	+	+	✓	✓
Missing	✗	+	✓	✓	+	+	✓	✓	✓
Misoriented	✗	+	✓	+	+	+	✓	✓	✓
Insuff/Excess	✓	+	✗	✓	✗	✗	✗	✗	+
Component Reliability	✗	✗	✗	✗	✗	✗	✗	✗	✓

FIGURE 2: Test coverage of the different testers.

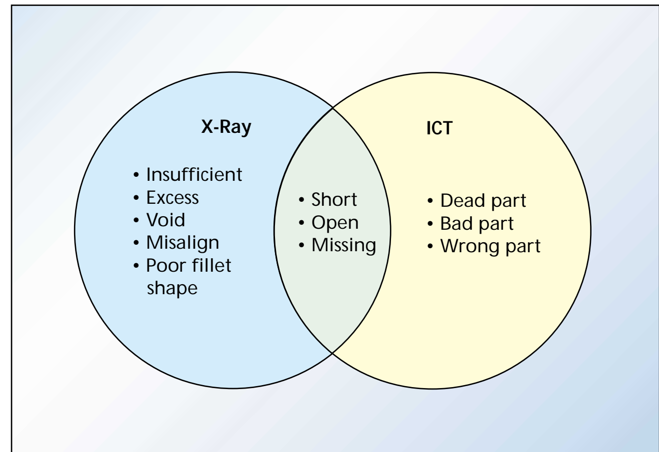


FIGURE 3: Overlapping and complementary test coverage of the AXI/ICT strategy.

different test approaches would make optimizing a test strategy very difficult and time consuming.

Based on this prediction model and the test coverages shown in Figure 2, a common test strategy for high-complexity boards is to use a combination of AXI, ICT and FT. AXI tests the structural integrity of the solder joints, ICT tests the electrical integrity of the components and PCB, and functional test verifies the PCB's performance characteristics. In addition, depending on customer requirements, some type of ESS testing may also be performed. The main objective of this combined test approach is to have as high a test coverage as possible, while using tests that have complementary test coverage (Figure 3).

On complex boards, typically about 80 to 90 percent of all defects found are structural or process defects. AXI provides about 95 percent coverage of these structural defects. Therefore, using AXI before ICT and functional test results in a significant reduction in the defects found at ICT and functional test. In addition, AXI pinpoints the exact location of the defects. As a result, the repair cost at AXI is low while the time to complete the repair is fast.

Without AXI as the initial screen, hours would be needed to debug the defective boards at ICT and FT, due to their high complexity. Relying on ICT and FT to catch the defects would lead to high work-in-process, extremely high cycle times and very poor process-throughput and asset utilization, due to their retest/debug/repair loops.

Combined Test Benefits

AXI/ICT/FT test methods are highly complementary and ensure the highest test coverage on high-complexity boards, independent of any test access and new packaging technology. The benefits of this strategy are:

• Faster time to market occurs because of the faster prototype testing. Close to 95 percent test coverage of structural defects can be tested within hours of application development, as opposed to days for an ICT test approach.

• The highest quality of boards shipped is ensured.

• Reduced costs at ICT, FT and ESS occur through reduced debug and repair by catching the structural defects at x-ray and repairing these with minimal debug cost.

• Shorter product cycle times and improved asset utilization occur through reduced retest/debug/repair loops at ICT/FT and ESS.

The net effect of this combined test strategy for complex boards is a lower overall cost of test, debug and repair.

By far the most important benefit of using this combined test strategy is the impact on time-in-process or cycle time. This combined test strategy results in boards being processed substantially faster than by using traditional test methods. For complex boards, this test strategy helps shorten the overall time-in-process by a factor of three through reduced time in debug and repair. Thus, the combined test method dramatically improves asset utilization and inventory turns.

Implementation Issues

A significant benefit of using AXI in the combined test approach is that the manufacturer can achieve close to 100-percent fault coverage on structural defects within hours of application development as opposed to days for other test methods.

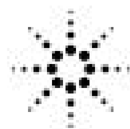
Most companies have experience with ICT and functional test, but few have extensive experience with x-ray test. As with ICT, AXI takes considerable investment in resources and training to ensure high quality and rapid x-ray test.

One issue often overlooked is design-for-test (DFT) for structural test. Unlike electrical tests, structural test systems focus on testing the physical structure of the board, its joints and components. Therefore, a different set of DFT issues come to light. For example, the consistency of pad geometry layouts for the same part type on all product families is a key issue in ensuring rapid test development. Without this consistency, application development times can triple or quadruple, and application false fail rates and false accept rates will be less than optimal.

Conclusion

In today's business environment, manufacturers must continuously drive down costs while coping with increased product complexity and shorter product life cycles. The complexity and time-to-market pressures make high-complexity boards particularly difficult to manufacture. To ensure the optimal test strategy, the proprietary QMS tool helps determine test strategy on a case-by-case basis. Because 80 to 90 percent of all defects on high-complexity boards are generally structural in nature, automated inspection tools like AOI and AXI should be complemented with ICT, FT and ESS methods. This combined test approach greatly reduces time-in-process by minimizing time spent in debug/repair/retest loops. ■

***Amit Verma** is a structural test engineer, e-mail: averma@celestica.com; **Mark Ogden** is the manager of structural test engineering, e-mail: mogden@celestica.com; and **John Kokoska** is a structural test engineer, e-mail: jkokoska@celestica.com; all with Celestica Inc., Toronto, Canada.*



Agilent Technologies

Innovating the HP Way

5988-0528EN

Copyright ©2000 by **CMP Media Inc.**, 600 Community Drive, Manhasset, NY 11030.
Reprinted with permission from Circuits Assembly, August 2000.
www.circuitsassembly.com